IN THE CLAIMS

We claim:

1. A method, comprising:

etching a recess into a substrate, the recess having a bottom;

implanting an ionized species into the bottom of the recess to form an amorphous etch stop region, the ionized species being electrically neutral within the substrate; and

etching the substrate with an anisotropic wet etch.

2. The method of claim 1, wherein the ionized species is an element that is the same as the substrate.

3. The method of claim 2, wherein the substrate is silicon and wherein the element is silicon.

4. The method of claim 1, wherein the ionized species has a low solubility in the substrate.

5. The method of claim 4, wherein the ionized species has an ionic radius greater than 130 pm or an ionic radius less than 80 pm.

6. The method of claim 4, wherein the ionized species is a noble element.

7. The method of claim 1, wherein the substrate is a single crystal with a vertical [100] crystal plane, a horizontal [110] crystal plane, and diagonal [111] crystal plane and

wherein etching the single crystal with the alkaline anisotropic wet etch causes faceting along the [111] crystal plane relative to the [100] crystal plane.

8. The method of claim 7, wherein the alkaline anisotropic wet etch solution has a pH of approximately 10 or higher.

9. The method of claim 7, wherein the alkaline anisotropic wet etch does not include an oxidizer.

10. The method of claim 1, wherein implanting an element into a substrate to form an amorphous etch stop region comprises a dose of the element in the approximate range of $5 \times e^{14}$ atoms/cm^2 and $1 \times e^{15}$ atoms/cm^2.

11. The method of claim 1, wherein implanting an ionized species into a substrate to form an amorphous etch stop region comprises an implant energy within the approximate range of 1 KeV and 20 KeV.

12. The method of claim 1, wherein etching the recess into the substrate comprises an anisotropic dry plasma etch.

13. A method comprising:

implanting an ionized species into a substrate to form an amorphous etch stop region, the ionized species being electrically neutral within the substrate;

etching a recess into a substrate; and

etching the substrate with an anisotropic wet etch.

14. The method of claim 13, wherein implanting the recess with the ionized species comprises a dose of the ionized species in the approximate range of e^{15} atoms/cm^2 and 1 x e^{16} atoms/cm^2.

15. The method of claim 13, wherein implanting the recess with the ionized species comprises an implant energy within the approximate range of 10 KeV and 40 KeV.

16. A method comprising:

forming a gate and a pair of sidewall spacers on either side of the gate above a single-crystal silicon substrate having a vertical [100] crystal plane, a horizontal [110] crystal plane, and a diagonal [111] crystal plane;

etching a recess in the single-crystal silicon substrate along the vertical [100] crystal plane with an anisotropic dry plasma etch;

implanting silicon into the bottom of the recess to form an amorphous etch stop;

etching the recess along the diagonal [111] crystal plane with an anisotropic wet etch having a pH of at least approximately 10 and no oxidizer; and

filling the recess with an electronically doped silicon germanium material to form a source/drain region.

17. The method of claim 16, further comprising a source/drain tip implant region under the sidewall spacers.

18. The method of claim 16, further comprising a shallow trench isolation region comprising an oxide and wherein the anisotropic wet etch does not etch the shallow trench isolation region or a hardmask protecting the gate.

19. The method of claim 16, wherein filling the recess with an electronically doped silicon germanium material forms an epitaxial source/drain tip extension region underneath the gate.

20. A method comprising:

providing a substrate having a crystal lattice; and

disrupting the crystal lattice of the substrate with an ionized species that is electrically neutral within the substrate to form an etch stop region.

21. The method of claim 20, wherein disrupting the crystal lattice of the substrate comprises disrupting chemical bonds within a crystal plane of the crystal lattice.

22. The method of claim 20, wherein disrupting the crystal lattice comprises a combination of acceleration energy, ionic radius, and mass of the element that is sufficient to disrupt chemical bonds of the crystal lattice.

23. A structure comprising:

a substrate having a plurality of vertical [100] crystal planes, a plurality of horizontal [110] crystal planes, and a plurality of diagonal [111] crystal planes, the substrate having a recess shaped as an inverse truncated pyramid having four walls along four diagonal [111] planes and a flat bottom along a horizontal [110] plane; and

an amorphous etch stop region containing an electrically neutral element within the substrate in the flat bottom of the recess, wherein the amorphous etch stop region acts as a mask to protect the substrate surface.

24. The structure of claim 23, wherein the substrate is single-crystal silicon.

25. The structure of claim 24, wherein the element is silicon.

26. The structure of claim 23, wherein the recess has an aspect ratio within the approximate range of 1:1 and 1:5.

27. The structure of claim 23, further comprising a cantilever protruding out over the recess.

28. A transistor, comprising:

a crystalline semiconductor substrate having a plurality of vertical [100] crystal planes, a plurality of horizontal [110] crystal planes, and a plurality of diagonal [111] crystal planes;

a gate electrode formed above the crystalline semiconductor substrate;

a pair of sidewall spacers, one on each side of the gate electrode; and

a pair of source/drain regions, one source/drain region under each of the sidewall spacers and wherein the source/drain regions are defined by the bottom of the spacers and by the diagonal [111] crystal planes.

29. The structure of claim 28, wherein the pair of source/drain regions extend beneath the pair of sidewall spacers by a distance of up to the width of one of the pair of sidewall spacers.

30. The structure of claim 28, wherein the pair of source/drain regions extend under the gate electrode by a distance in the approximate range of 10% and 20% of the width of the gate electrode.